ABSTRACT OF THE DISCLOSURE

In a memory cell array, a floating-gate field-effect transistor connected to a word line and a bit line is disposed in a matrix configuration. The floating-gate field-effect transistor is composed of a source and a drain formed inside a P-type well provided inside an N-type well on a P-type semiconductor substrate, a floating gate formed over between the source and the drain with a tunnel oxide interposed therebetween, and a control gate formed on the floating gate with an interlayer insulating film interposed therebetween. When an erasing pulse is applied, a voltage of 6V is applied to the P-type well with use of a first high-voltage pumping circuit, while a voltage of 9V is applied to the N-type well with use of a second high-voltage pumping circuit. This makes it possible to provide a highly reliable nonvolatile semiconductor memory device capable of preventing occurrence of latchup.